JARS - Task #967

Milestone # 128 (New): PRUEBAS DE DISEÑO

Test de adquisición para envío de varios IPP's

05/13/2017 11:11 PM - John Rojas

Status:	Closed	**Start date:**	09/21/2017
Priority:	Normal	**Due date:**	09/26/2017
Assignee:	John Rojas	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	Versión 2.0	**Spent time:**	0.00 hour

Description

History

#1 - 05/17/2017 09:58 PM - John Rojas

- Subject changed from Test de adquisición con NTX>1 to Test de adquisición para envío de varios IPP's

- Due date changed from 05/18/2017 to 05/22/2017

#2 - 05/29/2017 03:04 AM - John Rojas

- Due date changed from 05/22/2017 to 06/08/2017

- Start date changed from 05/16/2017 to 06/06/2017

#3 - 05/29/2017 05:28 AM - John Rojas

- Start date changed from 06/06/2017 to 06/07/2017

#4 - 06/26/2017 03:33 PM - John Rojas

- Due date changed from 06/08/2017 to 07/14/2017

- Start date changed from 06/07/2017 to 07/12/2017

#5 - 08/23/2017 04:18 AM - John Rojas

- Parent task changed from #197 to #128

#6 - 08/23/2017 05:18 AM - John Rojas

- Due date changed from 07/14/2017 to 09/15/2017

- Start date changed from 07/12/2017 to 09/13/2017

#7 - 09/26/2017 01:14 PM - John Rojas

- Due date changed from 09/15/2017 to 09/26/2017

- Status changed from New to In progress

- Start date changed from 09/13/2017 to 09/21/2017

- % Done changed from 0 to 90

- 25/09/2017: Se creó el bloque gen_cr_signals.vhd en el FPGA de Control para simulación de señales SYNC y WIN del CR y comportamiento cuando se envían varios IPP's. Conexión con la tarjeta Bus para generación y envío de datos a la tarjeta de Control.

#8 - 10/25/2017 03:09 AM - John Rojas

- Status changed from In progress to Resolved

- % Done changed from 90 to 100

#9 - 11/29/2017 06:56 PM - John Rojas

- Status changed from Resolved to Closed