JARS - Task #181

Milestone # 127 (New): TEST DE DESCRIPCIÓN Y VERIFICACIÓN DE HARDWARE (TESTBENCH)

Implementar testbench de protocolo LVDS (programación y control)

10/28/2015 02:05 PM - John Rojas

Status:	Closed	**Start date:**	01/27/2016
Priority:	Normal	**Due date:**	01/28/2016
Assignee:	John Rojas	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	Versión 2.0	**Spent time:**	0.00 hour

Description

History

#1 - 11/18/2015 12:39 PM - Joaquín Verástegui

- Target version set to Versión 2.0

#2 - 11/19/2015 03:01 PM - John Rojas

- Due date set to 12/27/2015

- Start date changed from 10/28/2015 to 12/07/2015

#3 - 11/19/2015 03:17 PM - John Rojas

- Due date changed from 12/27/2015 to 01/31/2016

- Start date changed from 12/07/2015 to 01/04/2016

#4 - 01/26/2016 08:55 AM - John Rojas

- Due date changed from 01/31/2016 to 01/28/2016

- Start date changed from 01/04/2016 to 01/27/2016

#5 - 02/09/2016 04:32 PM - John Rojas

- Status changed from New to Resolved

- % Done changed from 0 to 100

- 28/01/2016: Se simuló la comunicación del FPGA de Control y el FPGA de Programación para la recepción de comandos a través de LVDS, utilizando los sub-bloques cmd_mux y lvds_tx_prog en el FPGA de Control y lvds_rx_prog y cmd_demux en el FPGA de Programación.

#6 - 05/28/2017 12:44 AM - John Rojas

- Status changed from Resolved to Closed