JARS - Task #165

Milestone # 124 (New): DESCRIPCION DE HARDWARE

Integrar firmware del bloque de programación y LVDS

10/28/2015 10:54 AM - John Rojas

Status:	Closed	**Start date:**	01/18/2016
Priority:	Normal	**Due date:**	01/21/2016
Assignee:	John Rojas	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	Versión 2.0	**Spent time:**	0.00 hour

Description

History

#1 - 10/28/2015 10:54 AM - John Rojas

- Parent task set to #124

#2 - 11/18/2015 12:48 PM - Joaquín Verástegui

- Target version set to Versión 2.0

#3 - 11/18/2015 05:10 PM - John Rojas

- Due date set to 01/10/2016

- Start date changed from 10/28/2015 to 12/28/2015

#4 - 01/26/2016 08:47 AM - John Rojas

- Due date changed from 01/10/2016 to 01/21/2016

- Status changed from New to Resolved

- % Done changed from 0 to 100

- 21/01/16: Se implementó el bloque LVDS de recepción del bloque de del FPGA de Control. Con el testbench se complementa la verificación funcional de esta parte.

#5 - 01/26/2016 10:42 AM - John Rojas

- Start date changed from 12/28/2015 to 01/18/2016

#6 - 05/17/2017 10:13 PM - John Rojas

- Status changed from Resolved to Closed