JARS - Task #160

Milestone # 124 (New): DESCRIPCION DE HARDWARE

Implementar comunicación UDP en FPGA

10/28/2015 10:38 AM - John Rojas

Status:	Closed	**Start date:**	09/28/2015
Priority:	Normal	**Due date:**	10/11/2015
Assignee:	John Rojas	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	Versión 2.0	**Spent time:**	0.00 hour

Description

History

#1 - 11/05/2015 09:54 AM - John Rojas

- % Done changed from 0 to 70

#2 - 11/17/2015 08:23 AM - John Rojas

- Status changed from New to In progress

- % Done changed from 70 to 80

#3 - 11/18/2015 12:10 PM - John Rojas

- Due date set to 10/11/2015

- Start date changed from 10/28/2015 to 09/28/2015

#4 - 11/18/2015 12:48 PM - Joaquín Verástegui

- Target version set to Versión 2.0

#5 - 01/18/2016 08:49 AM - John Rojas

- 18/01/16: Se tiene implementado la comunicación con la PHY y se está trabajando en el manejo del bloque de control.

#6 - 01/18/2016 08:52 AM - John Rojas

- Status changed from In progress to Closed

- % Done changed from 80 to 100