JARS - Task #158

Milestone # 124 (New): DESCRIPCION DE HARDWARE

Implementar protocolo entre FPGA's de transferencia y control

10/28/2015 10:36 AM - John Rojas

Status:	Closed	**Start date:**	08/31/2015
Priority:	Normal	**Due date:**	09/13/2015
Assignee:	John Rojas	**% Done:**	100%
Category:		**Estimated time:**	32.00 hours
Target version:	Versión 2.0	**Spent time:**	0.00 hour

Description

History

#1 - 10/28/2015 10:45 AM - John Rojas

- Subject changed from Implementar comunicación LVDS entre FPGA's to Implementar protocolo entre FPGA's de transferencia y control

#2 - 11/18/2015 11:08 AM - John Rojas

- Due date set to 09/13/2015

- Status changed from New to Closed

- Start date changed from 10/28/2015 to 08/31/2015

Se implementó los bloques para la comunicación entre los FPGA´s de transferencia y control.

#3 - 11/18/2015 12:48 PM - Joaquín Verástegui

- Target version set to Versión 2.0

#4 - 11/19/2015 02:32 PM - John Rojas

- Estimated time set to 32.00 h