JARS - Task #152

Milestone # 123 (New): ESTUDIOS PREVIOS

Revisar protocolo de comunicación LVDS en FPGA

10/28/2015 09:51 AM - John Rojas

Status:	Closed	**Start date:**	08/03/2015
Priority:	Normal	**Due date:**	08/23/2015
Assignee:	John Rojas	**% Done:**	100%
Category:		**Estimated time:**	0.00 hour
Target version:	Versión 2.0	**Spent time:**	0.00 hour

Description

History

#1 - 10/28/2015 10:33 AM - John Rojas

- Assignee set to John Rojas

#2 - 11/05/2015 09:50 AM - John Rojas

- % Done changed from 0 to 80

#3 - 11/18/2015 12:48 PM - Joaquín Verástegui

- Target version set to Versión 2.0

#4 - 11/18/2015 03:14 PM - John Rojas

- Due date set to 08/23/2015

- Status changed from New to Resolved

- Start date changed from 10/28/2015 to 08/03/2015

- % Done changed from 80 to 100

#5 - 01/05/2016 08:32 AM - John Rojas

- Status changed from Resolved to Closed