Development of a radio mode for the long wavelength array (LWA) receiving system to study the equatorial aeronomy

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Abstract

Instituto Geofísico del Perú (IGP), through its scientific facility at the Jicamarca Radio Observatory (JRO), monitors the upper atmosphere with different instruments: radars, GNSS receivers, magnetometers, among others. Through a National Science Foundation (NSF) MRI award, two Long Wavelength Array (LWA) receiving stations will be installed at 50 km south (Santa María) and 170 km east (Huancayo) of Jicamarca. Each station is composed of 256 dual-polarization antennas circularly distributed with a diameter of 100 m. In this poster, we present the development of the radio receiver mode for the Long Wavelength Array (LWA). The receiver consists of 16 AMD Zynq UltraScale+ MPSoC ZCU102 devices and 128 ADS5296A ADCs, configured for 12-bit resolution with a sampling rate of 160 MSPS.

1. Introduction

Implementing a tristatic radar system at Jicamarca would enhance different types of observations, requiring the establishment of two receiving stations near IGP-JRO. The receiving stations of Santa María and Huancayo would enable independent, passive radio astronomy observations. Furthermore, the combined stations would provide 3D Doppler information. To expand the capabilities to monitor the equatorial ionosphere, we are building a radio receiver mode for the Long Wavelength Array (LWA).

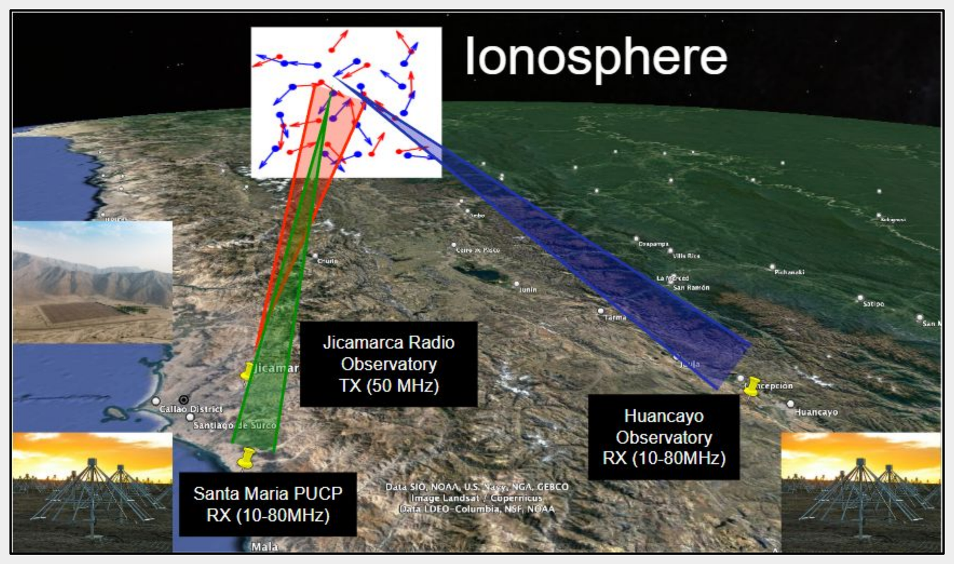

Figure 1. Tristatic radar system at Jicamarca.

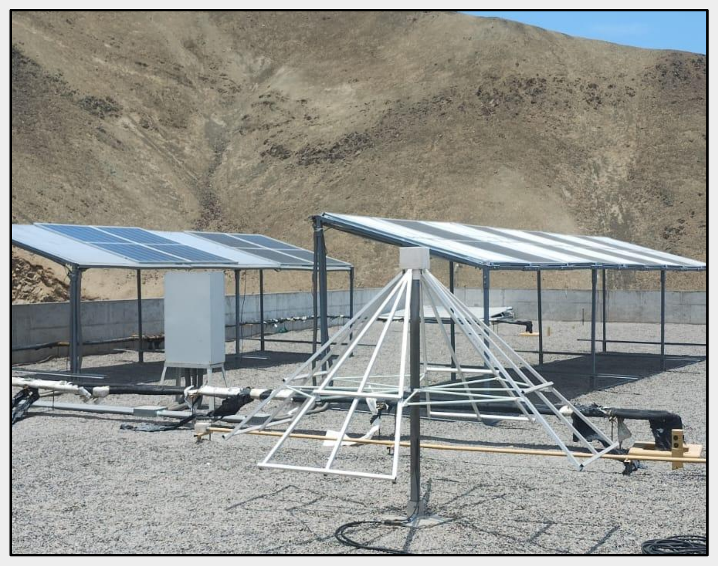

Figure 2. LWA Antenna.

2. FPGA internal architecture

The hardware synthesis was based on the VHDL hardware description language, using a behavioral description style for the modules, such as the SPI controller, register map, numerically controlled oscillator (NCO), demodulator, DSP, beamforming, and data transfer. Additionally, the Arm Cortex-A53 integrated into the ZCU102 was also used for register writing through the SPI protocol.

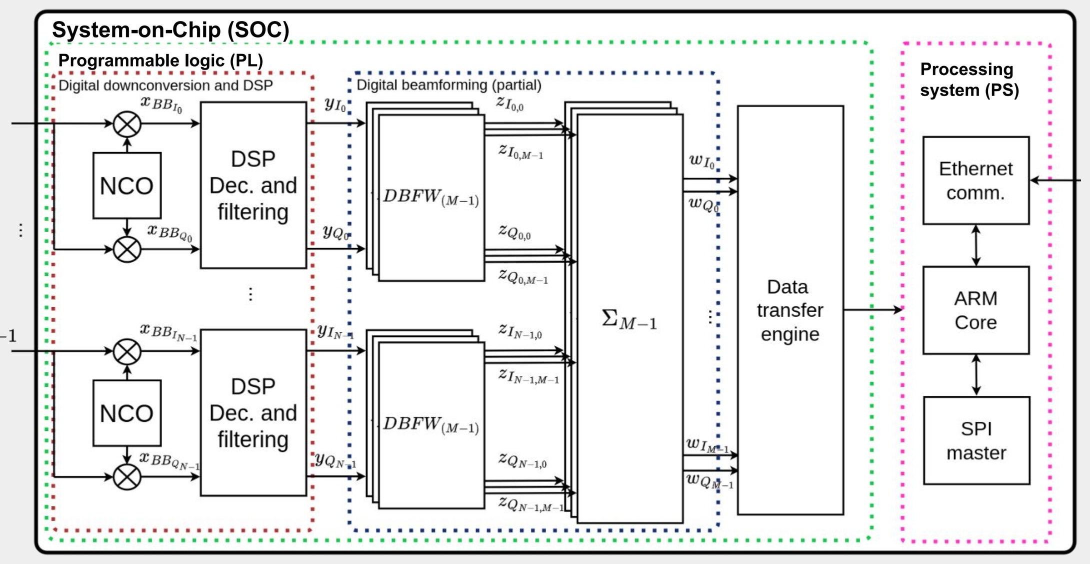

Figure 3. Block design.

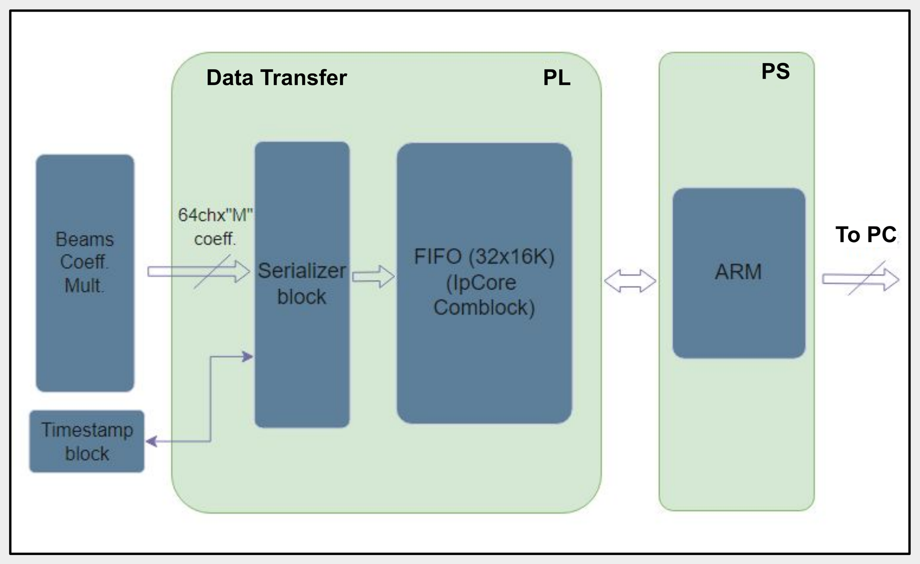

Figure 4. Data transfer module.

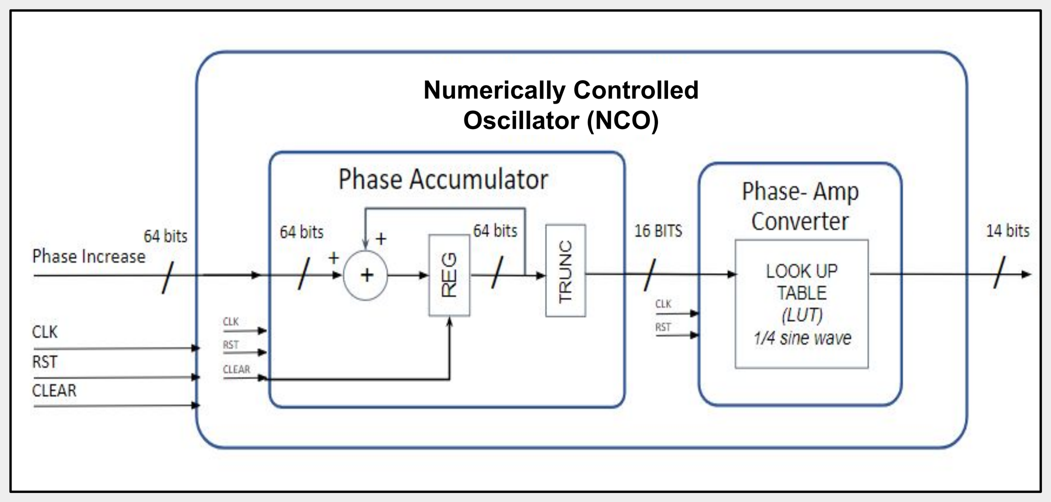

Figure 5. Numerically controlled oscillator.

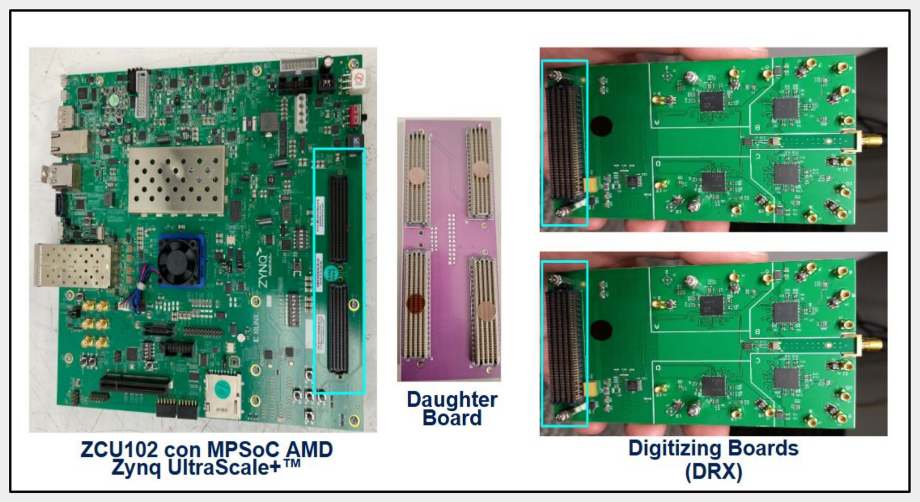

Figure 6. LWA Hardware.

3. Results

We tested the developed receiver using a testbench in the Xilinx–AMD Vivado development environment. Due to delays in the manufacturing of the digitizer board (DRX), initial experiments were conducted using the Red Pitaya Signal Lab 250-12 platform, where the hardware descriptions of the DSP modules were evaluated. Additionally, the system supports the demodulation of radio frequency signals from 1 MHz to 80 MHz from other radars. This work focuses on the characterization and processing of signals at 49.92 MHz and 32.5 MHz, that corresponds to the operational frequencies of the Jicamarca and SIMONe radars.

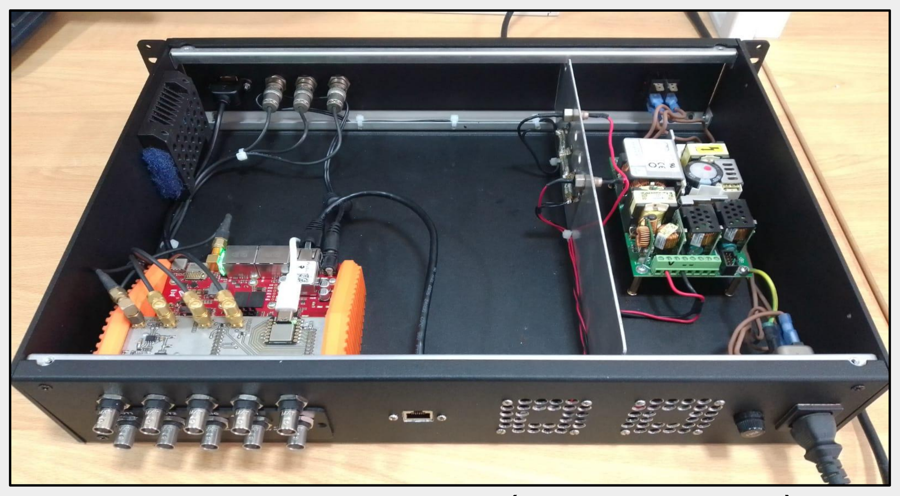

Figure 7. Hardware for test *(Red Pitaya 250-12)*.

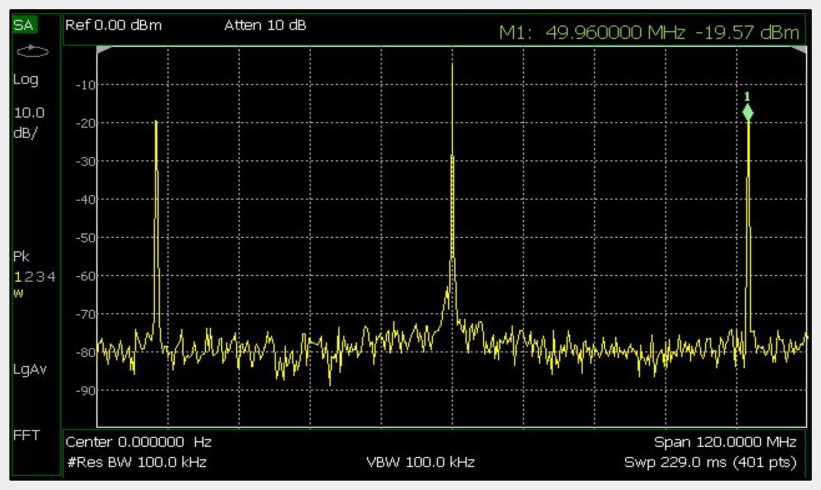

Figure 8. 49.96 MHz input signal to the ADCs.

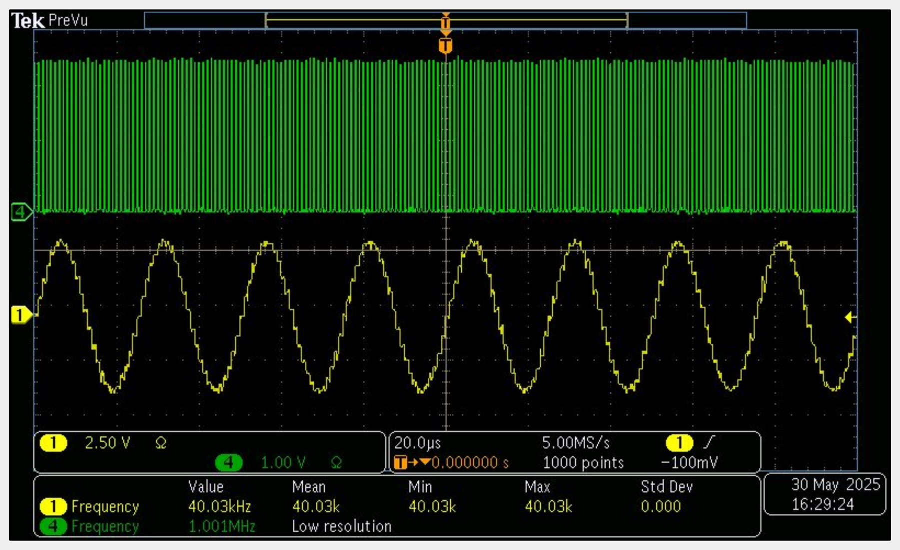

Figure 9. 40 KHz Doppler signal in time.

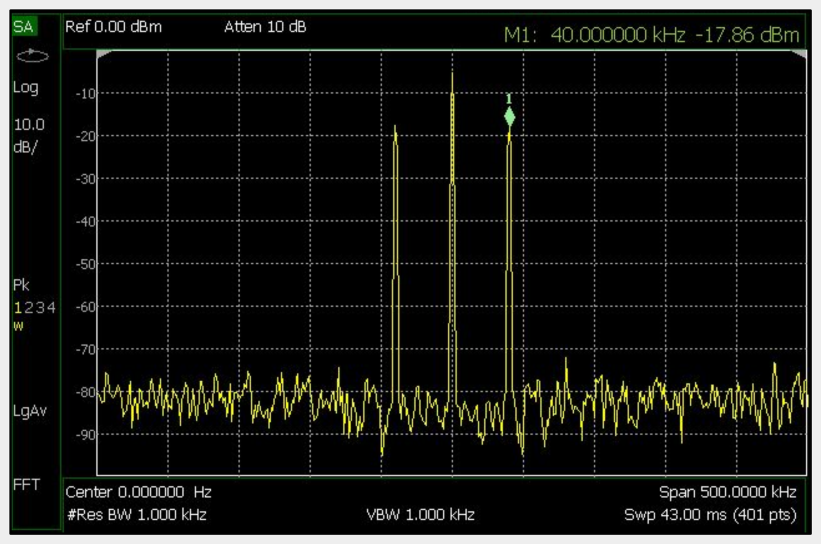

Figure 10. 40 KHz Doppler signal in spectrum.

4. Future Work

- The next step involves integrating all the mentioned modules and the IP Core Clocking Wizard using the structural description style in Vivado.
- Subsequently, the ADS5296A ADCs will undergo evaluation using the copper ball experiment, followed by the initial data acquisition tests at the IGP-JRO facilities.

5. Acknowledgments

The Jicamarca Radio Observatory is a facility of the Instituto Geofisico del Peru operated with support from the NSF AGS-2213849 through Cornell University. We also thank the support of Ciencia Internacional, a Peruvian non-profit civil association that supports the operation of the IGP-JRO.

6. References

[1] B. Estalla (2023), Development of a radiofrequency signal generator for ionosonde radar transmitter using low-cost SDR.

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