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FEATURES

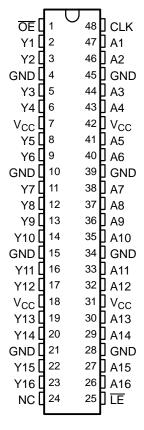
- Member of the Texas Instruments Widebus™
 Family
- Ideal for Use in PC100 Register DIMM
- Operates From 1.65 V to 3.6 V
- Max t_{nd} of 3.8 ns at 3.3 V
- ±12-mA Output Drive at 3.3 V
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- Designed to Comply With JEDEC 168-Pin and 200-Pin SDRAM Buffered DIMM Specification
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This 16-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when the latch-enable (\overline{LE}) input is low. When \overline{LE} is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If \overline{LE} is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC - No internal connection

The outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T _A	PAC	KAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	SSOP - DL	Tube	SN74ALVC162334DL	- ALVC162334	
40°C to 95°C	330P - DL	Tape and reel	SN74ALVC162334DLR		
-40°C to 85°C	TSSOP - DGG	Tape and reel	SN74ALVC162334DGGR	ALVC162334	
	TVSOP - DGV	Tape and reel	SN74ALVC162334DGVR	VC2334	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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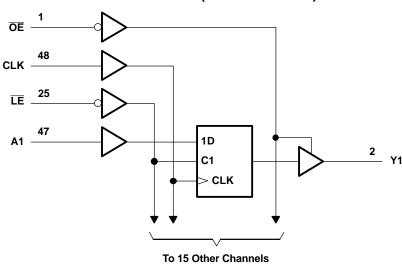


FUNCTION TABLE

	INPUTS								
ŌĒ	LE	CLK	Α	Y					
Н	Χ	X	Χ	Z					
L	L	X	L	L					
L	L	X	Н	Н					
L	Н	1	L	L					
L	Н	1	Н	Н					
L	Н	L or H	Χ	Y ₀ ⁽¹⁾					

(1) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)





SN74ALVC162334 16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V_{CC}	Supply voltage range		-0.5	4.6	V	
VI	Input voltage range ⁽²⁾		-0.5	4.6	V	
V_{O}	Output voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V		
I _{IK}	Input clamp current	V ₁ < 0		-50	mA	
I _{OK}	Output clamp current	V _O < 0		-50	mA	
Io	Continuous output current		±50	mA		
	Continuous current through each V _{CC} or GN	ID		±100	mA	
		DGG package		70		
θ_{JA}	Package thermal impedance (4)	DGV package		58	°C/W	
		DL package		63		
T _{stg}	Storage temperature range		-65	150	°C	

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
VI	Input voltage		0	3.6	V
Vo	Output voltage	0	V _{CC}	V	
		V _{CC} = 1.65 V		-2	
	IPak Israel autout assessed	V _{CC} = 2.3 V		-6	A
I _{OH}	High-level output current	V _{CC} = 2.7 V		-8	mA
		V _{CC} = 3 V		-12	
		V _{CC} = 1.65 V		2	
	Low lovel output ourrest	V _{CC} = 2.3 V		6	A
l _{OL}	Low-level output current	V _{CC} = 2.7 V		8	mA
		V _{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V	
T _A	Operating free-air temperature		-40	85	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

³⁾ This value is limited to 4.6 V maximum.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

Р	ARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP(1) MAX	UNIT		
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2			
		$I_{OH} = -2 \text{ mA}$	1.65 V	1.2			
	V _{OH}	$I_{OH} = -4 \text{ mA}$	2.3 V	1.9			
V_{OH}		L 6 mA	2.3 V	1.7	V		
		I _{OH} = -6 mA	3 V	2.4			
		$I_{OH} = -8 \text{ mA}$	2.7 V	2			
		I _{OH} = -12 mA	3 V	2			
		I _{OL} = 100 μA	1.65 V to 3.6 V	0.2			
		I _{OL} = 2 mA	1.65 V	0.45			
		I _{OL} = 4 mA	2.3 V	0.4			
V_{OL}		L 6 mA	2.3 V	0.55	V		
		I _{OL} = 6 mA	3 V	0.55			
		I _{OL} = 8 mA	2.7 V	0.6			
		I _{OL} = 12 mA	3 V	0.8			
I		V _I = V _{CC} or GND	3.6 V	±5	μΑ		
loz		$V_O = V_{CC}$ or GND	3.6 V	±10	μΑ		
I _{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	40	μΑ		
ΔI_{CC}		One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V	750	μΑ		
<u> </u>	Control inputs	V V or CND	221/	5	~F		
Ci	Data inputs	$V_{I} = V_{CC}$ or GND	3.3 V	5.5	pF		
Co	Outputs	$V_O = V_{CC}$ or GND	3.3 V	7.5	pF		

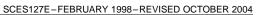
⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				V _{CC} =	V _{CC} = 1.8 V		2.5 V .2 V	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency				(1)		150		150		150	MHz	
t Pulse duration	LE low		(1)		3.3		3.3		3.3		20		
t _w	Pulse duration	CLK high or low	CLK high or low			3.3		3.3		3.3		ns	
		Data before CLK↑		(1)		1.4		1.7		1.5			
t _{su}	Setup time	Data before LE ↑	CLK high	(1)		1.2		1.6		1.3		ns	
		Data before LET	CLK low	(1)		1.4		1.5		1.2			
		Old time Data after CLK↑ Data after EE↑ CLK high or low		(1)		0.9		0.9		0.9			
t _h	поій шпе			(1)		1.1		1.1		1.1		ns	

⁽¹⁾ This information was not available at the time of publication.





SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V_{CC} = 2.5 V \pm 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INPOT)	(OUTPUT)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			(1)		150		150		150		MHz
	Α			(1)	1	4.4		4.5	1.1	3.9	
t _{pd}	ĪĒ	Υ		(1)	1	5.8		6	1.3	5	ns
	CLK			(1)	1	5.2		5.4	1	4.9	
t _{en}	ŌĒ	Y		(1)	1	6.4		6.4	1.1	5.4	ns
t _{dis}	ŌĒ	Y		(1)	1	4.7		5.1	1.7	5	ns

⁽¹⁾ This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

from 0° C to 65° C, $C_{L} = 50 \text{ pF}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1	UNIT	
	(51)	(6611 61)	MIN	MAX	
t _{pd}	Α	Y	1.2	3.8	20
	CLK	Y	1.1	4.8	ns

OPERATING CHARACTERISTICS

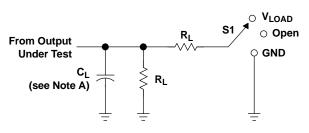
 $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT	
	Power dissipation	Outputs enabled	$C_1 = 0$. $f = 10 \text{ MHz}$	(1)	31	36	, r
C_{pd}	capacitance	Outputs disabled	$C_L = 0$, $f = 10 \text{ MHz}$	(1)	7	11	p⊦

⁽¹⁾ This information was not available at the time of publication.



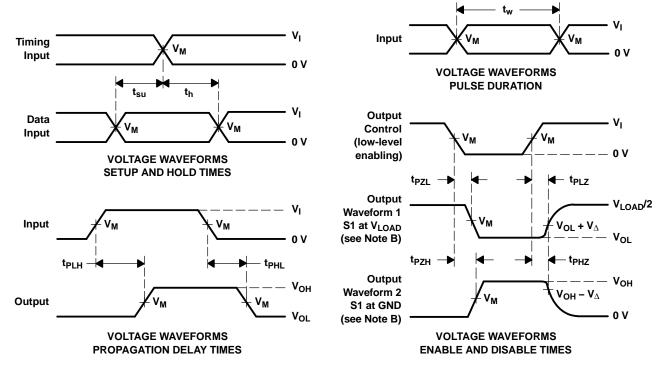
PARAMETER MEASUREMENT INFORMATION



TEST	S 1
t _{pd}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

V	INPUT		V	v		В	V
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	$oldsymbol{V}_\Delta$
1.8 V	V _{CC}	≤ 2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V \pm 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{Ω} = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms







PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVC162334DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVC162334DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVC162334DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVC162334DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVC162334DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVC162334DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC162334DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC162334DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC162334DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVC162334DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

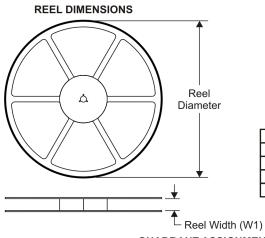
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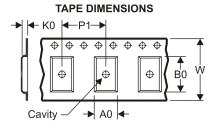
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PACKAGE MATERIALS INFORMATION

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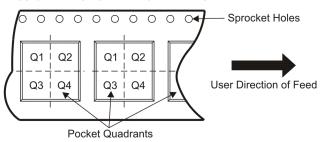
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

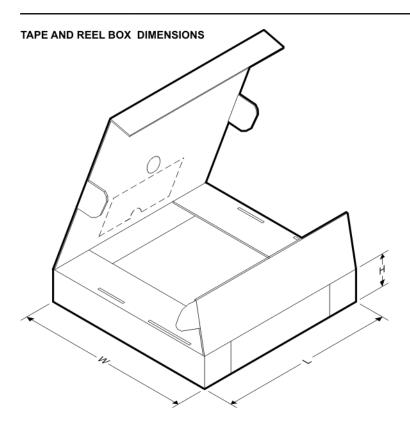
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVC162334DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ALVC162334DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74ALVC162334DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

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*All dimensions are nominal

7 il difficiolo die fiorilita										
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)			
SN74ALVC162334DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0			
SN74ALVC162334DGVR	TVSOP	DGV	48	2000	346.0	346.0	33.0			
SN74ALVC162334DLR	SSOP	DL	48	1000	346.0	346.0	49.0			

DL (R-PDSO-G**)

48 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194



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